Gate Capacitance-Dependent Field-Effect Mobility in Solution-Processed Oxide Semiconductor Thin-Film Transistors

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Solution-processed oxide semiconductors (OSs) used as channel layer have been presented as a solution to the demand for flexible, cheap, and transparent thin-film transistors (TFTs). In order to produce high-performance and long-sustainable portable devices with the solution-processed OS TFTs, the low-operational voltage driving current is a key issue. Experimentally, increasing the gate-insulator capacitances by high-*k* dielectrics in the OS TFTs has significantly improved the field-effect mobility of the OS TFTs. But, methodical examinations of how the field-effect mobility depends on gate capacitance have not been presented yet. Here, a systematic analysis of the field-effect mobility on the gate capacitances in the solution-processed OS TFTs is presented, where the multiple-trapping-and-release and hopping percolation mechanism are used to describe the electrical conductivity of the nanocrystalline and amorphous OSs, respectively. An intuitive single-piece expression showing how the field-effect mobility depends on gate capacitance is developed based on the aforementioned mechanisms. The field-effect mobility, depending on the gate capacitances, of the fabricated ZnO and ZnSnO TFTs clearly follows the theoretical prediction. In addition, the way in which the gate insulator properties (e.g., gate capacitance or dielectric constant) affect the field-effect mobility maximum in the nanocrystalline ZnO and amorphous ZnSnO TFTs are investigated.

1. Introduction

Solution-processed oxide semiconductors (OSs) have received much attention due to their ability to produce transparent thin-film transistors (TFTs) on flexible substrates cheaply, which is a key in switching components for next generation displays such as smart windows, transparent mobile displays, and electronic papers.[1–9] Recently, high-quality OS films on plastic substrates have been successfully fabricated by developing low-temperature and solution-based processes (e.g., combustion process,[3] 'sol-gel on chip' process,[4] and photochemical activation methods[5]). These methods can accelerate the adoption of flexible OS TFTs to practical applications.

While the novel OS film-fabricating techniques are important, raising drive currents in low-operating voltages is also critical for low-power consuming and high-performance OS TFTs.[10–13] One of the conventional strategies to increase the drain current (I_D) for transistors is to increase the gate-insulator capacitances (C_i) based on the relationship of $I_D \propto C_i$ from the metal-oxide-semiconductor field-effect transistors (MOSFETs) theory.[14] Empirically, such strategies has been applied to solution-processed OS TFTs. However, the enhanced behaviors of I_D in the OS TFTs are quite different to that in MOSFETs,[3,5,10–13] since disordered metal ions or dense grain boundaries in the solution-processed OSs make the field-effect mobility (μ_{FE}) of the OS TFTs depend on the total number of accumulated charge carriers in the channel.[15,16] Therfore, μ_{FE} depends on C_i, and I_D is not in a linear relationship to C_i. The relationship between C_i and μ_{FE} is important for low-voltage and high-performance solution-processed OS TFTs. Futhermore, theoretical predictions for the device performances can be essential guidelines for designing and optimizing integrated TFT circuits.

The solution-processed OS disordering states can be categorized with nanocrystalline and amorphous states, which is determined by the number of metal elements that compose the OS films. Binary oxide systems (number of metal elements = 1) such as ZnO, InO_2, and SnO_2, have nanocrystalline states,[6,7,12,13] while the ternary or quaternary oxide systems (number of metal elements > 1) like ZnSnO, InZnO, and InGaZnO have the amorhpous phases.[3,5,8] In the experiment, both nanocrystalline and amorhpous OS TFTs by engineering C_i differ in electron-transporting mechanisms, but follow two

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features: under high-C_i conditions, maximum μ_{FE} values of OS TFTs can be achieved with lower gate voltages than with low-C_i conditions. This means that the sub-threshold swing value is reduced by increasing C_i.[3,5,10–13] For example, by replacing SiO_2 (C_i = 10.8 nF cm^{-2}) with ion-gel (C_i = 5.08 μF cm^{-2}) for gate insulating materials, 14.8 cm^2 V^{-1} s^{-1}μ_{FE} for solution-processed ZnO TFTs were demonstrated below the operating voltage of ≈3 V while the SiO_2-gated solution-processed ZnO TFTs operated over 10 V.[13] Additionally, the maximum μ_{FE} of the OS TFTs with high-k insulators is higher than that with low-k insulators within associated gate-bias ranges for device operations.[3,5,10,12] The photo-annealed InGaZnO TFTs on Al_2O_3 gate insulator (C_i = 138 nF cm^{-2}) showed 9.74 cm^2 V^{-1} s^{-1} for maximum μ_{FE} within gate-bias ranges < 10 V, while that on SiO_2 (C_i = 17 nF cm^{-2}) showed 2.64 cm^2 V^{-1} s^{-1} for maximum μ_{FE} within gate-bias ranges < 30 V.[5] Although these demonstrations have experimentally shown the enhanced performances of the solution-processed OS TFTs, a systematic analysis about the C_i increasing μ_{FE} for low voltage operations has not been intensively performed. In addition, the effect of gate-insulator perperties (e.g., capacitance or dielectric constant) on the maximum μ_{FE} of the devices has not been investigated.

Here, we systematically analyze the C_i–dependent μ_{FE} of a theoretical model representative of the solution-processed OS TFTs, where the electrical conductivity is based on the multiple-trapping-and-release (MTR) mechnism for the nanocrystalline OSs or the hopping percolation mechanism for the amorhpous OSs. For both theoretical models, we derive a single-piece analytic expression, which intuitively shows how the field-effect mobility and operational gate voltages can be determined by the gate capacitance. The developed theoretical formula is successfully verified by the fabricated solution-processed ZnO or ZnSnO TFTs. At low-voltage operations of ≈ 4 V, the ZnO TFTs shows that its μ_{FE} changes from 0.066 to 6.01 cm^2 V^{-1} s^{-1} following $\mu_{FE} \propto C_i^{1.66}$, while the ZnSnO TFTs shows $\mu_{FE} \propto C_i^{0.41}$. Futhermore, we investigate how the device perperties (e.g., gate capacitances and dielectric constant of gate insulator) affect the maximum μ_{FE}.

2. Development of Analytical Models for Nanocrystalline and Amorphous OS TFTs

The solution-processed OSs have highly disordered states where the electrical conductivity (σ) is different compared to their crystalline states ($\sigma \propto n$, where n is the total charge-carrier density). In the solution-processed OSs, the electron transport is limited by dense localized states between energy gaps, although the large spherical S-orbital of metal ion provides an efficient electron-transporting path.[17,18] For the nanocrystalline OSs, the electrical conduction is mainly limited to the electron-trapping sites between nanocrystal-domain boundaries (see **Figure 1**a).[19] The electron-trapping sites in the nanocrystalline OSs are introduced by the dense localized states between the energy gaps where the electron transport has been described by the MTR mechanism.[15,16,19] In the MTR model, most of the free electrons are assumed to be trapped in the localized states and only a small fraction of the electrons hopping to the transport bands from the localized states by thermal energy contribute temporarily to electrical conductions (see Figure 1c). Assuming the localized state distribution below the transport bands are a single exponential density of states (DOS), σ for the nanocrystalline OSs can be expressed as[15,16]

$$\sigma = \sigma_0 \left(\frac{\sin(\pi T/T_0) n}{(\pi T/T_0) N_t^{tot}} \right)^{\frac{T_0}{T}} \quad (1)$$

where σ_0 is the conductivity prefactor, N_t^{tot} is the total number of localized states per unit volume, T_0 is the characteristic temperature of the localized states representing the width of the exponential distribution below the transport bands, and T is the temperature of the device.

On the other hand, the electron transport in the amorphous OSs is governed by the thermally activated electron hopping between adjacent metal ions that hold electrons (see Figure 1b). When an external electric field is applied to the amorphous OSs, the electrons flow by the hopping process along the percolating-conduction path lying on metal ions (See Figure 1d), which determine the electrical conductivity.[18,20] We refer to this amorphous OS mechanism as the "variable-range-hopping (VRH) percolation model". In the VRH percolation model, dense localized states directly represent the disordered metal ions, and σ for the amorphous OSs within the localized states that follow the exponential DOS can be expressed as[20,21]

$$\sigma = \sigma_0 \left(\frac{\sin(\pi T/T_0)(T_0/T)^4 n}{B_c (2\alpha)^3} \right)^{\frac{T_0}{T}} \quad (2)$$

where B_c, the critical number for percolation onset, is ≈ 2.8 in the three-dimensional amorphous system[20] and α is the effective overlap parameter for the electron-hopping process.

We assumed the following for Equation 1 and 2: 1) The single exponential DOS is given by $g(E) = (N_t^{tot}/k_B T_0)\exp(-E/k_B T_0)$, where E is the energy of the state and is a positive value with respect to the transport bands and the localized state density is zero above the transport bands: $g(E) = 0$ when $E < 0$.[15,20] 2) n is approximated to n_t,[15,20] and n_t is the charge-carrier density in the localized states given by[15,20]

$$n_t = \frac{N_t^{tot} \pi T/T_0}{\sin(\pi T/T_0)} \exp\left(\frac{-q\phi_F}{k_B T_0} \right) \quad (3)$$

where Φ_F is the Fermi potential that is positive with respect to the transport bands, k_B is the Boltzmann constant, and q is the electron charge. 3) When the device is turned on, the deep-localized states as oxygen vacancies are entirely filled up and the tail-localized states induced by disordered metal ions only influences electrical transport in the channel.[22] In both MTR and VRH percolation models, Equations 1 and 2 are valid in the range of $T < T_0$.[15,20]

Meanwhile, μ_{FE} is defined as

$$\mu_{FE} = \frac{L}{W C_i V_{DS}} \frac{\partial I_D}{\partial V_{GS}} \quad (4)$$

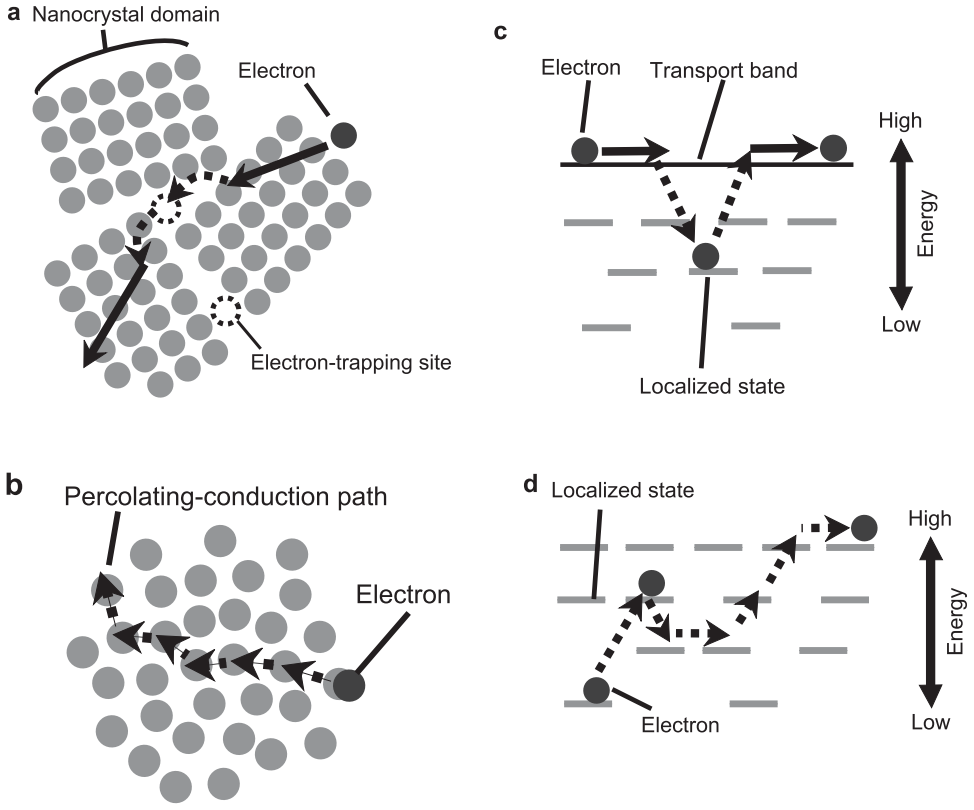

Figure 1. a,b) Schematic of electron-transporting principles for nanocrystalline (a) and amorphous (b) OSs. The orbitals of metal ions in the disordered OSs are illustrated by gray-colored circle, and oxygen ions are omitted for convenience. c,d) Schematic energy-band diagrams corresponding to the nanocrystalline (c) and the amorphous (d) OSs. In (a–d), the dash (or solid)-line arrows indicate thermally hopping (or freely moving) electron between disordered metal ions (or in nanocrystal domains).

in measured linear I_D–V_{DS} output-characteristic regimes where I_D is the electrical current passing through the drain electrode, V_{GS} (or V_{DS}) is the applied voltage between the gate (or drain) and the source electrode, and W and L are the width and length of the channel in the semiconductor film, respectively. In thin-film transistors, I_D can be determined by

$$I_D = \frac{W}{L}\int_0^{V_{DS}}\int_{\varphi_s}^{V_{ch}} \frac{\sigma}{(\nabla\varphi)_u}\exp\left(\frac{q(\varphi - V_{ch})}{k_B T}\right)d\varphi\, dV_{ch} \quad (5)$$

where φ is the electrostatic potential in the channel and subscript u depicts the normal direction vector component to the channel-gate insulator interface. The exponential term in the integral represents quasi-Fermi potentials in the OS film at non-equilibrium condition. φ_s is the electrostatic potential at the channel and gate insulator interface, which satisfies the boundary conditions given by $V_{GS} = V_{FB} + \varepsilon_0\varepsilon_s|(\nabla\varphi_s)_u|/C_i + \varphi_s$. In this case, V_{FB} is the flat-band voltage, ε_0 is the electrical permittivity in a vacuum, and ε_s is the relative permittivity of the OSs. We refer to φ_s as the surface potential of the channel. At the OS bulk, which is far from the channel-gate insulator interface, the electrostatic potential is $\varphi = V_{ch}$. $V_{ch} = V_{DS}$ is assumed to be at the drain electrode while $V_{ch} = 0$ is at the source electrode.[16]

After substituting Equation 1 (for the MTR model) or 2 (for the VRH percolation model) into Equation 5, taking the integral with mathematical manipulations using gradual channel approximation[14,16,23] leads to an explicit expression of I_D:

$$I_D = \sigma_0\delta\frac{W}{L}\frac{V_T}{\gamma - 1}\left(\sqrt{\frac{2\varepsilon_0\varepsilon_s k_B T_0 \sin(\pi T/T_0)}{q^2 N_t^{tot}\pi T/T_0}}\right)^{\gamma}\left(\frac{C_i}{\varepsilon_0\varepsilon_s}\right)^{\gamma-1} \times\left\{\left[\frac{V_{GS} - V_{FB} - \varphi_{sS}}{\gamma V_T} + \frac{\gamma}{\gamma - 1}\right]\left[\frac{V_{GS} - V_{FB} - \varphi_{sS}}{\gamma V_T}\right]^{\gamma-1} - \left[\frac{V_{GS} - V_{FB} - \varphi_{sD}}{\gamma V_T} + \frac{\gamma}{\gamma - 1}\right]\left[\frac{V_{GS} - V_{FB} - \varphi_{sD}}{\gamma V_T}\right]^{\gamma-1}\right\} \quad (6)$$

where $V_T = k_B T/q$ is the thermal voltage and $\gamma = 2T_0/T$. In Equation 6, I_D for the MTR model (or VRH percolation model) is calculated by taking $\delta = 1$ (or $\delta = [\pi(T_0/T)^3 N_t^{tot}/B_c(2\alpha)^3]^{(T_0/T)}$). φ_{sS} and φ_{sD} are the surface potential at the source and drain electrodes, respectively. These are expressed as

$$\varphi_{sS} = V_{GS} - V_{FB} - \gamma V_T W_0 \left[\sqrt{\frac{q^2 N_t^{tot}\pi T/T_0}{2\varepsilon_0\varepsilon_s k_B T_0 \sin(\pi T/T_0)}}\frac{\varepsilon_0\varepsilon_s}{C_i}\exp\left(\frac{V_{GS} - V_{FB} - \phi_F}{\gamma V_T}\right)\right] \quad (7\text{-}1)$$

and

$$\varphi_{sD} = V_{GS} - V_{FB} - \gamma V_T W_0 \left[\sqrt{\frac{q^2 N_t^{tot} \pi T/T_0}{2\varepsilon_0 \varepsilon_s k_B T_0 \sin(\pi T/T_0)}} \frac{\varepsilon_0 \varepsilon_s}{C_i} \exp\left(\frac{V_{GS} - V_{FB} - \phi_F - V_{DS}}{\gamma V_T}\right)\right] \quad (7\text{-}2)$$

where W_0 represents the principal branch of the Lambert Function.

Calculating μ_{FE} with Equation 6 and 7 yields

$$\mu_{FE} = \frac{\beta}{C_i}\left\{\left[\frac{qn_s}{\gamma V_T}\right]^{\gamma-1} - \left[\frac{qn_d}{\gamma V_T}\right]^{\gamma-1}\right\} \quad (8)$$

where n_s (or n_d) = $\varepsilon_0\varepsilon_s|(\nabla\varphi_{sS})_u|$ (or $\varepsilon_0\varepsilon_s|(\nabla\varphi_{sD})_u|$) is the accumulated charge carrier density at the source (or drain) electrodes and $\beta = \frac{\sigma_0\delta}{V_D(\gamma-1)}\left(\sqrt{\frac{2\varepsilon_0\varepsilon_s k_B T_0 \sin(\pi T/T_0)}{q^2 N_t^{tot}\pi T/T_0}}\right)^{\gamma}\left(\frac{1}{\varepsilon_0\varepsilon_s}\right)^{\gamma-1}$. Equation 8 reveals that raising the total number of charge carrier is important for high μ_{FE}, when the trap DOS in the OSs follows the exponential distributions. For the $V_{GS} - V_{FB} \geq V_{DS}$ region, the surface potentials can be approximated to $\varphi_{sS} \approx 0$ and $\varphi_{sD} \approx V_{DS}$.[16,23] In this case, n_s (or n_d) is written as n_s (or n_d) $\approx C_i(V_{GS} - V_{FB})/q$ (or $C_i(V_{GS} - V_{FB} - V_{DS})/q$) and Equation 8 is then expressed as

$$\mu_{FE} \cong \beta\left\{\left[\frac{V_{GS} - V_{FB}}{\gamma V_T}\right]^{\gamma-1} - \left[\frac{V_{GS} - V_{FB} - V_{DS}}{\gamma V_T}\right]^{\gamma-1}\right\} C_i^{\gamma-2} \quad (9)$$

which clearly shows how μ_{FE} can be determined by V_{GS} and C_i. To reach the equal-μ_{FE} value, high-C_i conditions require smaller V_{GS} than in low-C_i conditions. The validity of assumption in Equation 9 is discussed later in the paper. In addition, when we examine the C_i-dependent μ_{FE} with holding other device parameters, Equation 9 is reduced simply to

$$\mu_{FE} \cong \mu_{FE}^0\left(\frac{C_i}{C_i^0}\right)^{\gamma-2} \quad (10)$$

where μ^0_{FE} is the field-effect mobility at $C_i = C_i^0$. Equation 10 clearly shows that the μ_{FE} of nanocrystalline (or amorphous) TFTs strongly depend on the C_i variation. Increasing C_i results in increasing μ_{FE} in the same V_{GS} values.

3. Field-Effect Mobility Analysis Depending on Gate Capacitance using Model Devices

We first investigate how C_i affect the transfer characteristics of the MTR (or VRH percolation) model-based TFTs when the devices turn on (meaning the regime of $V_{GS} \geq V_{FB}$). According to Equation 6, the device characteristics of both TFT models are analogous to each other, so the MTR model is used to study the essential device physics. **Figure 2**a shows calculated I_D–V_{GF} ($V_{GF} = V_{GS} - V_{FB}$) transfer curves using Equation 6 for the device with various C_i (15 nF cm^{-2} to 240 nF cm^{-2}). Other device parameters are listed in **Table 1**. The calculated I_D–V_{GF} curves are representative of the solution-processed OS TFT transfer characteristics. The drain current transitions from a low V_{GF} to a high V_{GF} smoothly in log-scale.[3–13,16,24] By increasing C_i, I_D as a function of V_{GF} grows more rapidly within the V_{GF} region of 0 V < V_{GF} < 4 V. The sub-threshhold swing value, defined by $dV_{GF}/d(\log I_D)$, significantly decreases when just increasing C_i. Unlike conventional MOSFETs theory, the simulation results (or Equation 6) show that I_D of OS TFTs with the exponential trap DOS are in a nonlinear relationship with C_i (i.e., depends on $\approx C_i^{\gamma-1}$).

Figure 2b shows the calculated μ_{FE} as a function of C_i using Equation 8 at V_{GF} = 1, 2, and 4 V. All other device parameters are fixed as given in Table 1. μ_{FE} increases with increasing V_{GF}, which also describes well-known characteristics of the gate-bias-dependent μ_{FE} for the solution-processed OS TFTs.[4,11,24] μ_{FE} notably increases with increasing C_i within the C_i region of 10 nF cm^{-2} < C_i < 240 nF cm^{-2}. These calculated μ_{FE}–C_i characteristics closely follow the dotted lines plotted using Equation 9, indicating that μ_{FE} follows a power-law dependent on $C_i^{\gamma-2}$ shown in Equation 10. Since the surface potentials monotonically increases with increasing C_i, the μ_{FE}–C_i calculated curves slightly deviate from the dotted lines for the higher C_i. These small deviations are more obvious when V_{GF} approaches V_{DS}. However, the surface potential variations when C_i varies are not dominant enough to determine μ_{FE}. Therefore, the assumption in Equation 9 is still valid.

Using Equation 9, we also examine the relationship between C_i and V_{GF} when the μ_{FE} value is maintained. Figure 2c shows the C_i–V_{GF} characteristics under μ_{FE} = 0.1, 1, and 10 cm^2 V^{-1} s^{-1}. As expected, the μ_{FE} value under high-C_i conditions is easily

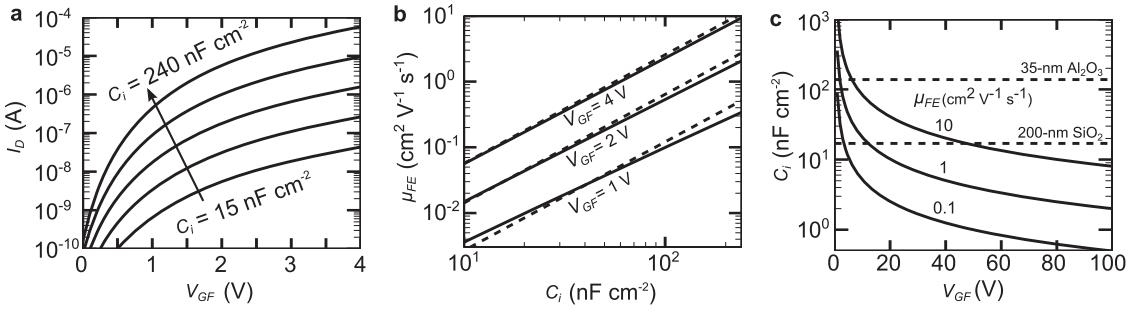

Figure 2. Calculated device performances on variation of the gate-insulator capacitance (C_i) for the MTR-model based TFTs. a) The calculated drain current (I_D) – V_{GF} [V_{GF} = the gate-source voltage (V_{GS})—the flat-band voltage (V_{FB})] transfer characteristics with varying C_i from 15 to 240 nF cm^{-2} (from bottom to top: 15, 30, 60, 120, 240 nF cm^{-2}), using Equation 6 with the parameters in Table 1. b) The calculated field-effect mobility (μ_{FE}) as a function of C_i using Equation 8 (solid lines) and Equation 9 (dash lines) for the case of a at V_{GF} = 1, 2, and 4 V. c) Calculated C_i–μ_{FE} characteristics under μ_{FE} = 0.1, 1, 10 cm^2 V^{-1} s^{-1}. The dash lines indicate the C_i values of 35-nm-thick Al_2O_3 (top) and 200-nm-thick SiO_2 (bottom) insulator.

Table 1. Device parameter values for the model devices in Figure 2.

Variables	Values	Units
W	1000	μm
L	50	μm
V_D	1	V
V_S	0	V
ε_s	7.5	–
T	293	K
T_0	535.5	K
N_t^{tot}	8.55×10^{-19}	cm^{-3}
σ_0	7.02	S cm^{-1}
Φ_F	0.2	eV

achieved with low-V_{GF} values. We assume that there are two types of solution-processed OS TFTs, for comparing the calculated C_i–V_{GF} characteristics with reported experimental results:[5] one with a 200 nm-thick SiO_2 (C_i = 17 nF cm^{-2}) layer for the gate insulator and the other with a 35 nm-thick Al_2O_3 (C_i = 138 nF cm^{-2}). To achieve μ_{FE} = 0.1 cm^2 V^{-1} s^{-1}, 4 V is sufficient as the maximum V_{GF} for both devices. When μ_{FE} = 1 cm^2 V^{-1} s^{-1}, the SiO_2 device requires 12 V for the V_{GF} while the Al_2O_3 device only needs 2 V. For higher μ_{FE} (>1 cm^2 V^{-1} s^{-1}), the required voltage values for the SiO_2 device are more increase than that for the Al_2O_3 device; When μ_{FE} is 10 cm^2 V^{-1} s^{-1}, the SiO_2 device requires V_{GF} = 47 V while the Al_2O_3 device requires only V_{GF} = 6 V. Meanwhile, these results suggest that ideal gate insulators, which is an perfect electrical insulating material (the dielectric-breakdown voltage is infinite, and the gate-leakage current at infinite V_{GF} is zero), can achieve any desired-μ_{FE} value with the required gate bias regardless of the C_i values. However, realistic gate insulator have non-zero gate-leakage currents and finite dielectric-breakdown voltages. In addition, the μ_{FE} increment is scattering-limited, which will be discussed in the experimental results. Therefore, a consideration for such aspect is necessary, although a simple examination of Equation 9 describes the possible low-voltage operation of the OS TFTs under high-C_i conditions.

4. Structure and Material Properties of Solution-Processed ZnO and ZnSnO TFTs

To verify this theoretical approach, we fabricated solution-processed OS TFTs based on a conventional bottom-gate top-contact structure with L of 1000 μm and W of 50 μm, as shown in **Figure 3**a. For the OS channel layer, solution-processed nanocrystalline ZnO (see Figure 3b) or amorphous ZnSnO (see Figure 3c) films were applied. The dielectric SiO_2 and amorphous $HfLaO_x$ layer thicknesses as gate insulators were tuned in order to change C_i. The capacitors of p-type $Si/SiO_2/HfLaO_x/Al$ were fabricated to characterize C_i and the SiO_2 and $HfLaO_x$ thickness in each capacitor is equal to that of the corresponding OS TFTs. The capacitors were designed in squares of 300 μm × 300 μm, the capacitances of which measured under AC bias with a frequency of 20 Hz vary from 13 nF cm^{-2} to 203 nF cm^{-2}. Due to a high dielectric constant and good insulating property of the amorphous $HfLaO_x$ layer,[25,26] the capacitors maintains a low dissipation factor of ~3% at 20 Hz. In all ZnO (or ZnSnO) TFTs, the $HfLaO_x$ layer ensured an equal interface between the gate insulator and ZnO (or ZnSnO) films. Other device fabrication details are provided in the Experimental Section.

5. Verification of a Single-Piece Formula for Gate Capacitance-Dependent Field-Effect Mobility using Solution-Processed ZnO and ZnSnO TFTs

To validate Equation 6, we measured both I_D–V_{DS} output and I_D–V_{GS} transfer characteristics of the ZnO TFTs (and ZnSnO TFTs) with C_i = 203 nF cm^{-2}. The measured experimental curves clearly fit Equation 6 (see Figure S1 in Supporting information), which validates that the developed theoretical model well describes the electron-transporting mechanisms of ZnO and ZnSnO TFTs. To plot the transfer characteristics for the devices on the I_D–V_{GF} axes, V_{FB} was determined by fitting the measured I_D–V_{GS} curves using Equation 6, with the device parameters depicted in **Table 2**. The I_D–V_{GS} curves for the ZnO TFTs (or ZnSnO TFTs) were fitted using the MTR (or VRH percolation) model. **Figure 4**a,b show the I_D–V_{GF} transfer characteristics for the ZnO and ZnSnO TFTs (symbols) at various C_i under V_{DS} = 1 V, respectively. The measured I_D–V_{GF} curves increase more rapidly for the device with the higher C_i within the region of 0 V < V_{GF} < 4 V for all solution-processed OS TFTs. This agrees with the theoretical predictions given in Figure 2a. Moreover, the measured I_D–V_{GF} curves obviously fit Equation 6 (solid lines in Figure 4a,b). T_0, N_t^{tot}, and σ_0 for the MTR model and T_0, N_t^{tot}, σ_0, α for the VRH percolation model, respectively, represent the essential physical properties of the

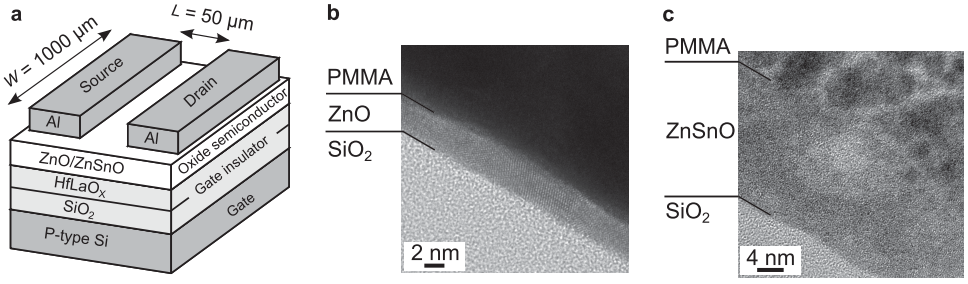

Figure 3. Structure and material properties of solution-processed OSs TFTs. a) Schematic structure of solution-processed ZnO (or ZnSnO) TFTs. b,c) Cross-sectional transmission electron microscope images of Si/SiO_2/ZnO (a) (or ZnSnO (b))/poly (methyl methacrylate) (PMMA) specimens.

ZnO and ZnSnO layers. Therefore, the results in Figure 4a (or 4b) suggest that i) the electronic structures of the ZnO (or ZnSnO) layer in all ZnO (or ZnSnO) devices are nearly identical and ii) the differences in the measured I_D between the ZnO (or ZnSnO) TFTs under the different-C_i conditions in Figure 4a (or 4b) arise entirely from the variation of C_i between the devices.

The fitted V_{FB} for the ZnO (or ZnSnO) TFTs varies from –0.96 V to 1.80 V (or from 0.12 V to 0.29 V). To prevent shifting V_{FB} by moisture adsorption and photo doping of the OS film,[27,28] the transfer characteristics were measured in a vacuum (~10^{-3} Torr) and in the dark, respectively. The work-function differences between the gate electrode and the ZnO (or ZnSnO) layer may be non-responsible to the variation of the fitted V_{FB}, since the physical properties of the ZnO (or ZnSnO) layer were almost equal and the gate electrode was a p-type Si for all devices. Therefore, the small differences in the fitted V_{FB} can be attributed to unintended oxide charges in the gate insulator.[14]

μ_{FE} for the ZnO (or ZnSnO) TFTs were calculated with $\gamma = 3.66$ (or $\gamma = 2.41$) at various V_{GF} in Equation 10 as shown in solid lines in **Figure 5**a (or 5b) (the measured μ_{FE} from the ZnO (or ZnSnO) TFTs with the lowest C_i was used as μ^0_{FE} and C_i^0). Figure 5 also shows the measured μ_{FE} for the ZnO and ZnSnO TFTs (symbols). In both cases, the measured μ_{FE}–C_i characteristics follow the solid lines calculated by Equation 11. This indicates that the μ_{FE} of the solution-processed OS TFTs follow a power-law dependence on $C_i^{\gamma-2}$, as discussed in this theoretical study. Thus, $\mu_{FE} \propto C_i^{1.66}$ for the ZnO TFTs and $\propto C_i^{0.41}$ for the ZnSnO TFTs. At low operating regions ($1\ V \le V_{GF} \le 4\ V$), μ_{FE} of both the ZnO and ZnSnO devices increases with increasing C_i (within the region of 13 nF cm^{-2} < C_i < 203 nF cm^{-2}). For the ZnO TFTs, notably, μ_{FE} is 0.066 cm^2 V^{-1} s^{-1} at C_i = 13 nF cm^{-2} and increases to 6.01 cm^2 V^{-1} s^{-1} at C_i = 203 nF cm^{-2} when V_{GF} is 4 V.

The increases in μ_{FE} can be explained by lowering the activation energy (E_a) of μ_{FE}. The most conventional method to derive E_a is to examine the T-dependent μ_{FE} using the Arrhenius equation ($\propto \exp(-E_a/k_BT)$).[15,16,19,20] By correlating Equation 10 to the Arrhenius equation, E_a for μ_{FE} can be expressed in terms of C_i as

$$E_a = E_a^0 - 2k_BT_0 \ln\left(\frac{C_i}{C_i^0}\right) \quad (11)$$

where E_a^0 is the activation energy at $C_i = C_i^0$. Equation 11 reveals that E_a monotonically decreases when C_i is increased. In both the MTR and VRH percolation models, the increment of C_i makes electrons rapidly fill the lower-lying localized states of the solution-processed OSs, which allows the additionally accumulating electrons to occupy the upper-lying localized states. Consequently, the electrons easily jump to the transport bands (for the MTR model) or neighboring localized states in the percolating path (for the VRH percolation model), which result in decreasing E_a and increasing μ_{FE}.

Although the fundamental electron-transporting mechanisms of both the amorphous and nanocrystalline OSs are different from each other, Equation 10 indicates that the μ_{FE} of both models depends on the C_i variation. Furthermore, Equation 10 explains that this dependency becomes stronger in the OSs with a higher T_0. In our results, μ_{FE} for the ZnO TFTs depend more on the variation of C_i than that for the ZnSnO TFTs, since T_0 for the ZnO TFTs is higher than that for the ZnSnO TFTs. These results correspond with previously reported studies which describe that the large 5S-orbitals of Sn-ions allow electron clouds to well overlap between adjacent metal ions in the ZnSnO amorphous system, and then the localized states have low electron-trapping energy.[29] In addition, the ZnSnO film was thermally annealed at 500 °C, which is higher than the annealing temperature for the ZnO film (300°C). Since high-temperature annealing makes the OSs film have denser packing structures,[18] it decreases the neighbor-to-neighbor distance between metal ions, which may decrease T_0. At a limit that satisfies $T \approx T_0$, μ_{FE} will not depend on C_i. This means that the limitations by the localized states in the electron transport are completely overcome by the thermal energy. Since our models are valid for $T < T_0$, Equation 10 cannot be applied to TFTs based on crystalline OSs ($T_0 \approx 0$) or TFTs under high-temperature operation ($T > T_0$).

For saturation mobility (μ_{Sat}) where the mobility is measured at saturated I_D–V_{DS} output regimes, an expression as a function of V_{GF} and C_i can be calculated from Equation 6 (see Equation S1 in Supporting information). The dependence of μ_{Sat} on C_i is equal to that for μ_{FE} since $\mu_{Sat} \propto C_i^{\gamma-2}$ according to Equation S1. An experimental investigation on μ_{Sat} will be conducted in future works, since this study only focuses on the field-effect mobility.

Table 2. Parameters for fitting Equation 6 to transfer characteristics of solution-processed OSs TFTs, and calculated conductivities of solution-processed OS layers.

Variables	MTR (for ZnO TFTs)		VRH percolation (for ZnSnO TFTs)		Units
Insulator	$HfLaO_x/SiO_2$	200-nm SiO_2	$HfLaO_x/SiO_2$	200-nm SiO_2	–
T_0	535.5 ± 0.4	538.1	353.5 ± 0.5	381.3	K
N_t^{tot}	8.55 ± 0.04 x 10^{18}	8.36×10^{18}	1.95×10^{19}	1.95×10^{19}	cm^{-3}
σ_0	7.02 ± 0.03	2.79	$1.10 \pm 0.08 \times 10^8$	5.75×10^8	S cm^{-1}
α	–		$9.42 \pm 0.41 \times 10^7$	9.56×10^7	cm^{-1}
σ[a)]	2.5×10^{-3}	1.0×10^{-3}	1.9×10^{-2}	4.0×10^{-2}	S cm^{-1}

[a)] σ for ZnO and ZnSnO layers in the devices were calculated using Equations 1 and 2, respectively.

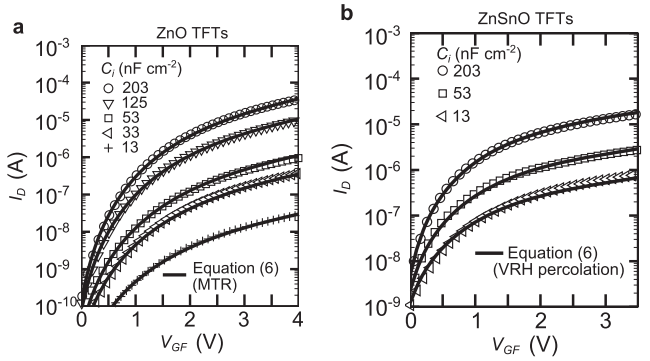

Figure 4. Transfer characteristics of the solution-processed OSs TFTs with various gate-insulator capacitances (C_i). a,b) The measured drain currents (I_D)–V_{GF} [V_{GF} = the gate-source voltage (V_{GS}) – the flat-band voltage (V_{FB})] transfer characteristics (symbols) of the ZnO (a) and ZnSnO (b) TFTs with various C_i from 13 nF cm^{-2} to 203 nF cm^{-2}, under a drain-source voltage (V_{DS}) of 1 V. Solid lines indicate theoretical fits to Equation 6. The MTR (or VRH percolation) model is used for the ZnO (or ZnSnO) TFTs.

6. Investigation of the Maximum Field-Effect Mobility of the ZnO and ZnSnO TFTs in Various Gate Insulator Properties

We next examine the maximum μ_{FE} of the devices under different-C_i conditions. The ZnO (or ZnSnO) TFTs with C_i = 13 and 203 nF cm^{-2} were selected, and the V_{GS} values for the devices were swept until the measured I_D were saturated (under V_{DS} = 1 V). **Figure 6** shows the measured μ_{FE} as a function of V_{GF}. The measured μ_{FE} for the ZnO TFT with C_i = 203 nF cm^{-2} (circle symbols in Figure 6a) rapidly increases and follows theoretical predictions (solid line) within V_{GF} < 3.8 V. It deviates the theoretical prediction for the region of V_{GF} > 3.8 V. The measured μ_{FE} has a maximum value of 7.93 cm^2 V^{-1} s^{-1} at V_{GF} = 5.7 V, which decreases for V_{GF} > 5.7 V. These mobility degradations are likely due to enhanced electron-to-electron or surface-roughness scattering effects at the $HfLaO_x$ and ZnO interfaces, since increased gate-electric fields make the channel electrons move toward the insulator/semiconductor interfaces.[30,31]

Meanwhile, the maximum μ_{FE} of the ZnO TFTs at C_i = 13 nF cm^{-2} (square symbols in Figure 6a) is smaller than that of the device with C_i = 203 nF cm^{-2}. In this case, the diminished μ_{FE} mainly arises from leakage currents, I_{leak}, flowing from gate to drain electrode (the current direction of I_{leak} is reverse to that of I_D). To examine the I_{leak} effect on the mobility, the measured μ_{FE} for total current, $I_{tot} = |I_D| + |I_{leak}|$, are also plotted and the field-effect mobility for the total current is referred to as μ^t_{FE}. As shown in Figure 6a, the differences between μ^t_{FE} (dash line) and μ_{FE} at C_i = 13 nF cm^{-2} are obvious, while μ^t_{FE} and μ_{FE} at C_i = 203 nF cm^{-2} are nearly equal. At V_{GF} = 47.7 V, the μ^t_{FE} at C_i = 13 nF cm^{-2} has the maximum value, which is comparable to the maximum μ_{FE} at C_i = 203 nF cm^{-2}. For the region where V_{GF} > 47.7 V, the μ^t_{FE} at C_i = 13 nF cm^{-2} also decreases due to the increased scattering effects. The detrimental effect of I_{leak} on the μ_{FE} becomes larger for the ZnO TFT with a single 200-nm-thick SiO_2 insulator (C_i = 17 nF cm^{-2}). In Figure 6a, the maximum μ_{FE} is 0.684 cm^2 V^{-1} s^{-1} as shown as triangles, while the maximum μ^t_{FE} is 4.19 cm^2 V^{-1} s^{-1}.

The measured I_{leak} comes from the gate insulator/the OSs junctions, since the currents for P-Si/gate insulator/Al structures are less than 10^{-9} A in the estimated voltage regions. The I_{leak} – V_{GS} characteristics are similar to that for diodes as I_{leak} turns on and increases only with positive bias for the gate electrode and negative bias for the semiconductors. I_{leak} may be related to the trap-assisted hopping in thermally grown SiO_2 and solution-processed $HfLaO_x$ (where the energy levels of the traps in the insulator are comparable to the mobile bands of the OSs), since the leakage current of the ZnO TFTs is very low with high quality SiO_2 that was grown by plasma-enhanced chemical vapor deposition methods.[31] We also found that the turn-on voltage of the I_{leak} depends on the gate insulator thickness, and that the dependence of I_{leak} on C_i is different to I_D, although detail mechanisms have not been investigated. In the case of the ZnO TFTs with C_i = 203 nF cm^{-2}, I_{leak} insignificantly affect until μ_{FE} reaches its scattering-limited maximum. However, I_{leak} for the ZnOs TFTs with C_i = 13 nF cm^{-2} is comparable to I_D at V_{GF} of ≈15 V, where μ_{FE} is only 1.3 cm^2 V^{-1} s^{-1}. In the case of the ZnO TFTs with the single 200-nm-thick SiO_2 insulator, I_{leak} is more quickly comparable to I_D than the device with C_i = 13 nF cm^{-2}, which severely disturbs μ_{FE} enough to make it increase.

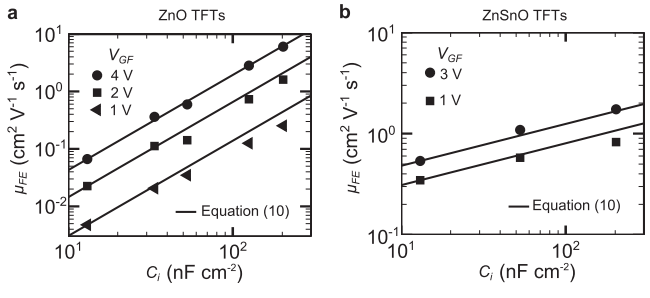

Figure 5. The measured field-effect mobility (μ_{FE}) depending on the gate-insulator capacitance (C_i) of the solution-processed OSs TFTs. a,b) The measured μ_{FE} – C_i characteristics (symbols) of the ZnO (a) and ZnSnO (b) TFTs under various V_{GF} [V_{GF} = the gate-source voltage (V_{GS}) – the flat-band voltage (V_{FB})]. Solid lines indicate theoretical results calculated using Equation 10. In (a,b), the drain-source voltage (V_{DS}) is 1 V.

However, the μ_{FE} – V_{GF} characteristics of the ZnSnO TFTs with 13 and 203 nF cm^{-2} are very similar to each other, as shown in Figure 6b. Since the energy depth of the localized states that correspond to T_0, is very small for the ZnSnO TFTs, the dependency of μ_{FE} on C_i is weak according to Equation 9. For the region of 0 V < V_{GF} < 6 V, the measured μ_{FE} for both devices have maximum values, and decrease according to the electron-scattering effect. Because I_{leak} is not dominant in the V_{GF} region, the measured μ_{FE} and μ^t_{FE} are almost identical for both devices. Such characteristics are also observed in the ZnSnO TFTs with single 200-nm-thick SiO_2 insulators, as shown in triangle symbols in Figure 6b; the trap-characteristic temperature is ~373 K and the differences between μ_{FE} and μ^t_{FE} can be ignored when 0 V < V_{GF} < 10 V.

The absence of I_{leak} effects (possible by reducing the source/drain electrode size or by replacing thermally grown SiO_2 with other high quality insulators)[31] show that the gate-insulator capacitance cannot be main factor that determines the maximum μ_{FE} of the solution-processed OS TFTs, but rather that

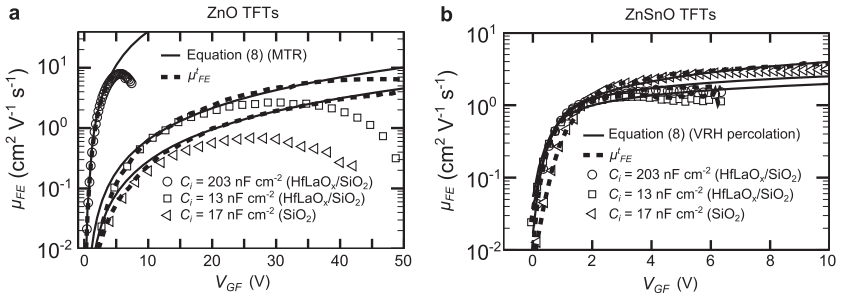

Figure 6. a,b) The measured field-effect mobility (μ_{FE}) as a function of V_{GF} [V_{GF} = the gate-source voltage (V_{GS}) – the flat-band voltage (V_{FB})] for the ZnO (a) and ZnSnO (b) TFTs. Solid lines indicate theoretical results using Equation 8; the MTR (or VRH percolation) model is used for the ZnO (or ZnSnO) TFTs. Dash lines indicate the field-effect mobility for the total current. In (a,b), the drain-source voltage (V_{DS}) is 1 V.

the physical properties of the gate insulator/OS interfaces are critical. The measured μ^t_{FE} of the ZnO TFTs perform better in HfLaO$_x$/ZnO interfaces than SiO$_2$/ZnO interfaces, while the ZnSnO TFTs show higher μ^t_{FE} values in SiO$_2$/ZnSnO interfaces than in HfLaO$_x$/ZnSnO interfaces. Additionally, we calculated the electrical conductivity of the ZnO (or ZnSnO) films in the devices by using Equation 1 (or 2) with the fitting parameters in Table 2. The calculated conductivity orders of magnitude are similar to the bulk conductivity of the solution-processed ZnO and ZnSnO films.[8,32] Meanwhile, the conductivities are affected by physical properties of the gate insulator/ZnO (or ZnSnO) interfaces in the devices. As a result, the ZnO (or ZnSnO) film conductivity at the HfLaO$_x$/ZnO (or ZnSnO) interfaces is higher (or lower) than that at the SiO$_2$/ZnO (or ZnSnO) interfaces, which is consistent with the result of the measured μ^t_{FE} in Figure 6. The high-dielectric environment by the gate insulator is not the dominant factor that determine the μ_{FE} in the channel (the dielectric constants of HfLaO$_x$ and SiO$_2$ are 22 and 3.9,[26] respectively), which has been known to decrease the Coulomb-scattering effects in a 2-dimensional semiconductor.[33] The root-mean-square surface roughness of SiO$_2$ and HfLaO$_x$ are similar when measured by an atomic force microscope.[26] We may conclude that getting good interfaces for high-μ_{FE} values depends on OS film-growing procedures on top of the gate insulator surfaces during the solution processes.

7. Conclusion

In conclusion, we investigated how C_i affects μ_{FE} of the solution-processed OS TFTs. With the developed TFT model based on the MTR and VRH percolation mechanisms, we successfully verified that μ_{FE} of the nanocrystalline ZnO and the amorhpous ZnSnO TFTs depends on the gate capacitances in the power-law dependence, which cannot be supported by the conventional MOSFETs theory. Also, the characteristics of the C_i-dependent μ_{FE} of the fabricated OS TFTs are clearly and well explained by the single-piece analytical expression. μ_{FE} of the ZnO TFTs which have the high-trap characteristic temperature strongly depends on C_i than that of the ZnSnO TFTs having the low-trap characteristic temperature. In particular, when the ZnO TFTs had different C_i, values from 13 to 203 nF cm^{-2}, the measured μ_{FE} dramatically changed by ≈100 times from 0.066 cm^2 V^{-1} s^{-1} at C_i = 13 nF cm^{-2} to 6.01 cm^2 V^{-1} s^{-1} at C_i = 203 nF cm^{-2} for a low-voltage operation (V_{GF} = 4 V). The measured μ_{FE} degradaed by the leakage current flowing from the gate to drain electrode, and the μ_{FE} degradation was more notable for the devices with low C_i and high T_0. Without the leakage current, the μ_{FE} of the ZnO and ZnSnO TFTs would have the scattering-limited maximum. Our findings can be the general guideline of the the C_i–dependent μ_{FE} characteristics for TFTs based on disordered semiconductors with single exponential DOS for the localized states, like organic semiconductors[21] as well as solution-processed OSs. The proposed single-piece expression for the field-effect mobility will be utilized to intuitively predict, design, and optimize solution-processed OS TFTs.

8. Experimental Section

All TFTs were fabricated on heavily B-doped p-type Si wafer substrates with a 8-nm, (for TFTs with C_i > 100 nF cm^{-2}), 50-nm (for TFTs with C_i = 53 nF cm^{-2}), 100-nm (for TFTs with C_i = 33 nF cm^{-2}), and 200-nm (for TFTs with C_i = 13 nF cm^{-2})-thick SiO$_2$ layer, which were sequentially washed with detergent, de-ionized water, acetone, and isopropyl alcohol and exposed to ultraviolet ozone for 30 min before depositing films. The substrates for each capacitor were equal to those of associated TFT devices. The HfLaO$_x$ layers were deposited onto the substrates by spin coating of mixed hafnium:lanthanum-precursor solution, which were prepared by a method described in ref. [26]. A thickness of the fabricated HfLaO$_x$ layer was varied from 45 nm to ≈ 90 nm, where the thickness was controlled by multiple spin-casting of the HfLaO$_x$ layer (the thickness of single HfLaO$_x$ layer with spin casting at 2000 rpm was ≈ 45 nm). A ZnO solution (which was prepared by dissolving 0.001 mole of zinc oxide (Sigma–Aldrich 99.999%) into 12 mL of ammonium hydroxide (aq) (Alfa Aesar, 99.9%)) or a ZnSnO solution (which was prepared by dissolving 0.15 M zinc acetate (Sigma Aldrich 99.99%), 0.225 M tin chloride (Sigma Aldrich 99.99%), an 0.15 M ethanolamine (Sigma Aldrich 99.5%) into 2-methoxyethanol) was spin coated onto the HfLaO$_x$-coated substrates under ambient conditions.[6,8] The ZnO (or ZnSnO)-deposited substrates were then annealed at 300 °C (or 500 °C) for 1 h in ambient. Then, 100-nm-thick Al electrodes were deposited on all devices via thermal evaporation at 10^{-6} Torr; the TFTs and capacitors were defined by the metal shadow masks.

The transfer characteristics for all the TFTs and the capacitance characteristics for all the capacitors were measured using an Agilent 4155B semiconductor parameter analyzer and Agilent 4284A precision LCR meter, respectively, at 10^{-3} Torr in the dark. Cross-sectional images of the TFTs were obtained via a TEM (JEM-2100F, JEOL), and the specimens for TEM measurement were prepared using a focused ion beam instrument (NOVA 600 NanoLab, FEI Company).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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